## Intel® Advisor

Vectorization Optimization and Thread Prototyping

Munara Tolubaeva Software Technical Consulting Engineer



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## Data-Driven Threading Design

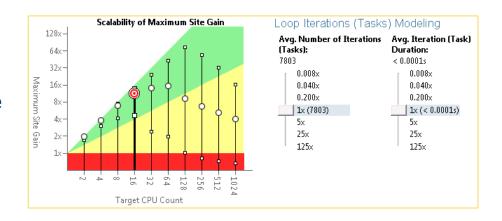
#### Intel® Advisor – Thread Prototyping

#### Have you:

- Tried threading an app, but seen little performance benefit?
- Hit a "scalability barrier"? Performance gains level off as you add cores?
- Delayed a release that adds threading because of synchronization errors?

#### Breakthrough for threading design:

- Quickly prototype multiple options
- Project scaling on larger systems
- Find synchronization errors before implementing threading
- Separate design and implementation -Design without disrupting development



Add Parallelism with Less Effort, Less Risk and More Impact

http://intel.ly/advisor-xe



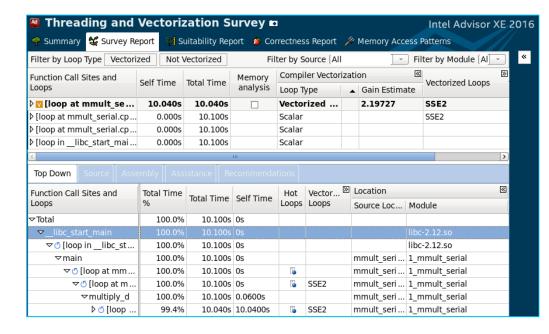
## Data Driven Vectorization Design

## Intel® Advisor – Vectorization Advisor Have you:

- Recompiled with AVX2, but seen little benefit?
- Wondered where to start adding vectorization?
- Recoded intrinsics for each new architecture?
- Struggled with cryptic compiler vectorization messages?

#### Breakthrough for vectorization design

- What vectorization will pay off the most?
- What is blocking vectorization and why?
- Are my loops vector friendly?
- Will reorganizing data increase performance?
- Is it safe to just use pragma simd?



**More Performance Fewer Machine Dependencies** 

## Factors that prevent Vectorizing your code

1. Loop-carried dependencies

```
DO I = 1, N
    A(I + M) = A(I) + B(I)
ENDDO
```

1.A Pointer aliasing (compiler-specific)

```
void scale(int *a, int *b)
{
   for (int i = 0; i < 1000; i++)
       b[i] = z * a[i];
}</pre>
```

2. Function calls (incl. indirect)

```
for (i = 1; i < nx; i++) {
   x = x0 + i * h;
   sumx = sumx + func(x, y, xp);
}</pre>
```

3. Loop structure, boundary condition

```
struct _x { int d; int bound; };

void doit(int *a, struct _x *x)
{
   for(int i = 0; i < x->bound; i++)
     a[i] = 0;
}
```

4 Outer vs. inner loops

```
for(i = 0; i <= MAX; i++) {
  for(j = 0; j <= MAX; j++) {
    D[j][i] += 1;
  }
}</pre>
```

5. Cost-benefit (compiler specific..)

And others.....



## Factors that slow-down your Vectorized code

1.A. Indirect memory access

```
for (i=0; i<N; i++)
A[B[i]] = C[i]*D[i]
```

1.B Memory sub-system Latency / Throughput

```
void scale(int *a, int *b)
{
   for (int i = 0; i < VERY_BIG; i++)
        c[i] = z * a[i][j];
        b[i] = z * a[i];
}</pre>
```

2. Small trip counts not multiple of VL

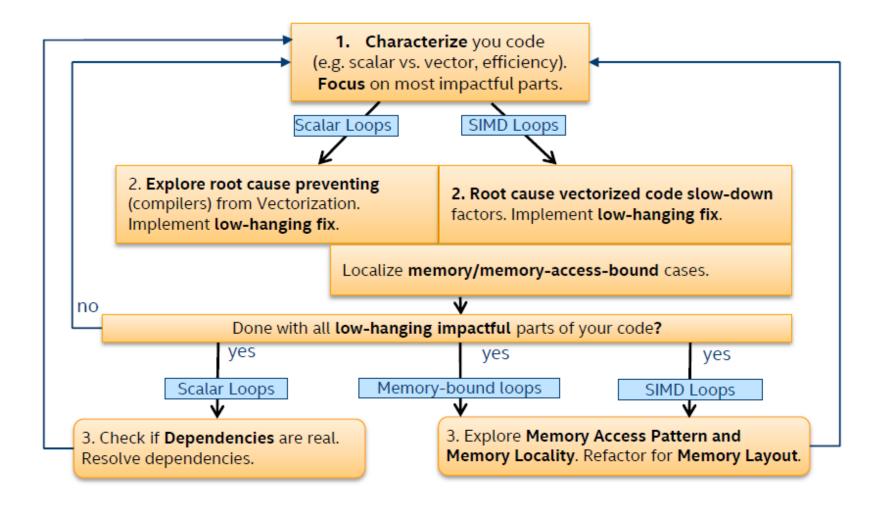
```
void doit(int *a, int *b, int
unknown_small_value)
{
  for(int i = 0; i <
  unknown_small_value; i++)
      a[i] = z*b[i];
}</pre>
```

3. Branchy codes, *outer vs. inner loops* 

5. MANY others: spill/fill, fp accuracy trade-offs, FMA, DIV/SQRT, Unrolling, even AVX throttling...

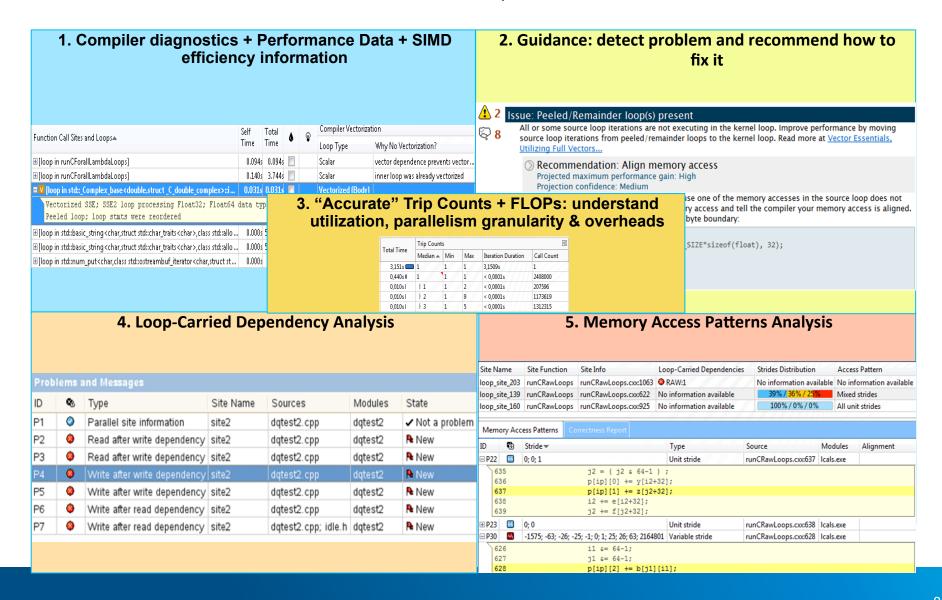
## Intel® Advisor helps you increase performance!

Recommended methodology



#### 5 Steps to Efficient Vectorization - Vector Advisor

(part of Intel® Advisor, Parallel Studio, Cluster Studio 2016)



## 1. Compiler diagnostics + Performance Data + SIMD efficiency information

	Function Call Sites and Loops▲	Self Time	Total Time	å	ନ୍ତ	Compiler Vectorization	
						Loop Type	Why No Vectorization?
	⊞ [loop in runCForallLambdaLoops]	0.0945	0.094s			Scalar	vector dependence prevents vector.
	⊞ [loop in runCForallLambdaLoops]	0.140s	3.744s			Scalar	inner loop was already vectorized
	■V [loop in std::_Complex_base <double,struct_c_double_complex>::i</double,struct_c_double_complex>		0.031s			Vectorized (Body)	
Vectorized SSE; SSE2 loop processing Float32; Float64 data type(s) having Divisions; Square Roots operations Peeled loop; loop stmts were reordered							Roots operations
	⊞ [loop in std::basic_string < char, struct std::char_traits < char>, class std::allo	0.000s	544.0			Scalar	nonstandard loop is not a vectoriza .
	⊞ [loop in std::basic_string < char, struct std::char_traits < char >, class std::allo	0.000s	544.0			Scalar	nonstandard loop is not a vectoriza .
	⊞ [loop in std::num_put <char,class st<="" std::ostreambuf_iterator<char,struct="" td=""><td>0.000s</td><td>0.234s</td><td></td><td></td><td>Scalar</td><td>nonstandard loop is not a vectoriza .</td></char,class>	0.000s	0.234s			Scalar	nonstandard loop is not a vectoriza .

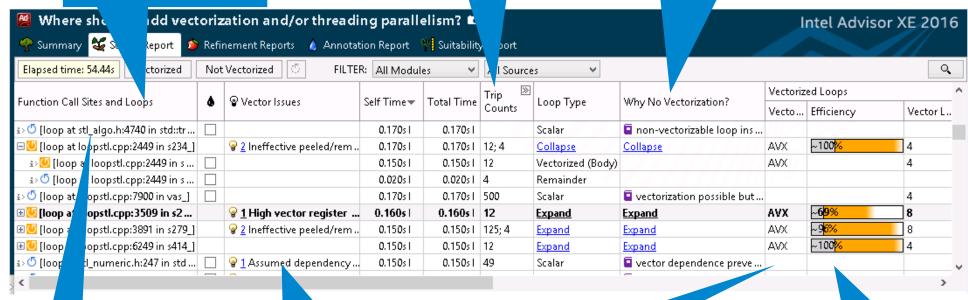
## The Right Data At Your Fingertips

Get all the data you need for high impact vectorization

Filter by which loops are vectorized!

Trip Counts

What prevents vectorization?



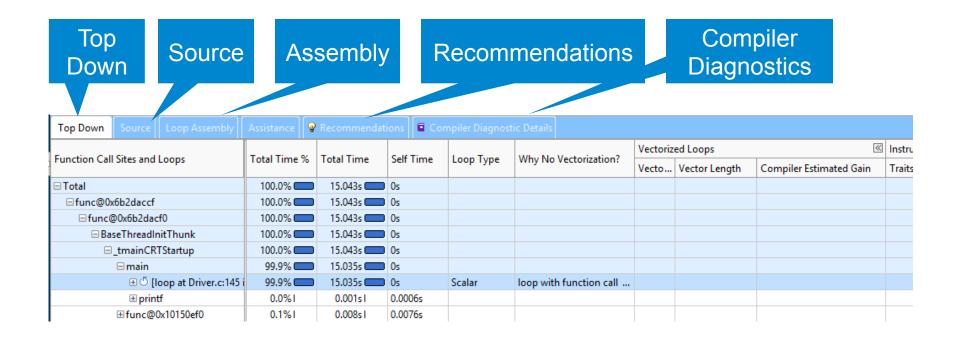
Focus on hot loops

What vectorization issues do I have?

Which Vector instructions are being use?

How efficient is the code?

#### All the data in one place



## Background on loop vectorization

A typical vectorized loop consists of

Main vector body

This is where we want our loops to be executing!

Fastest among the three!

Optional peel part

Used for the unaligned references in your loop. Uses Scalar or slower vector

Remainder part

Due to the number of iterations (trip count) not being divisible by vector length.
 Uses Scalar or slower vector.

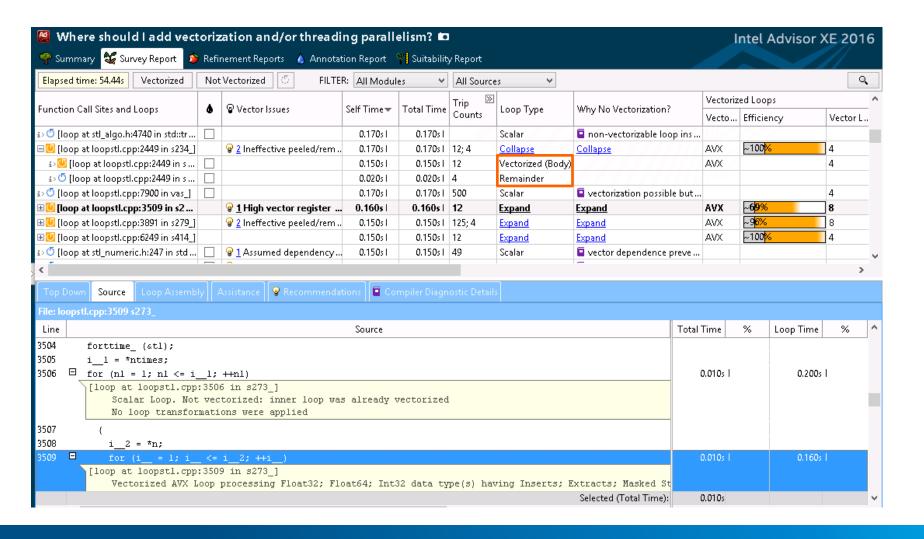
Larger vector register means more iterations in peel/remainder

- Make sure you Align your data!
- Make the number of iterations divisible by the vector length!



## Efficiently Vectorize your code

#### Intel Advisor – Vectorization Advisor



#### 1. Compiler diagnostics + Performance **Data + SIMD efficiency information**

Function Call Sites and Loops.	Self Time	Total Time	٥	0	Compiler Vectorization	
				¥	Loop Type	Why No Vectorization?
⊕ [loop in runCForallLambdaLoops]	0.094s	0.094s			Scalar	vector dependence prevents vector
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$\blacksquare \overline{\textbf{V}} \ [loop \ in \ std::\_Complex\_base < double, struct \_C\_double\_complex > ::$						
Vectorized SSE; SSE2 loop processing Float32; Float64 data type(s) having Divisions; Square Roots operations Peeled loop; loop stats were reordered						Roots operations
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#### 2. Guidance: detect problem and recommend how to fix it



#### 1 Issue: Peeled/Remainder loop(s) present



All or some source loop iterations are not executing in the kernel loop. Improve performance by moving source loop iterations from peeled/remainder loops to the kernel loop. Read more at Vector Essentials. Utilizing Full Vectors...

#### Recommendation: Align memory access

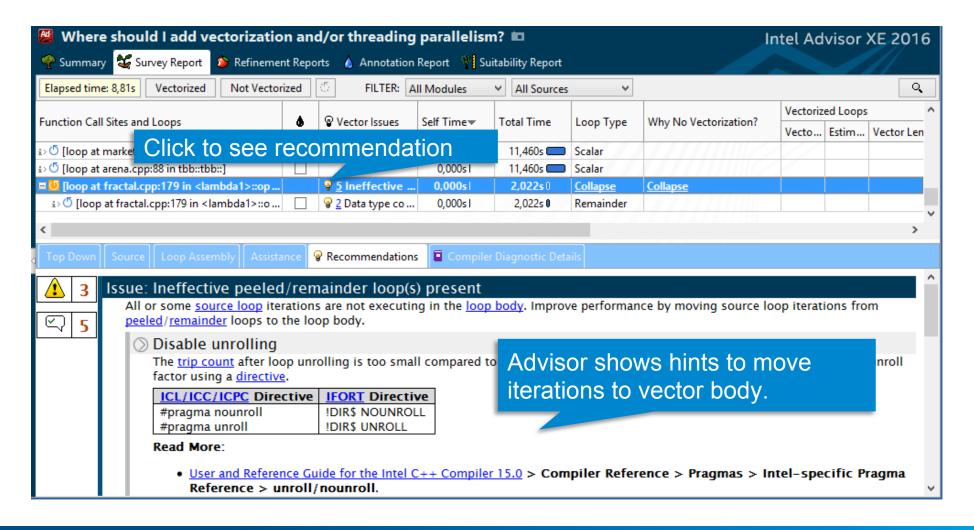
Projected maximum performance gain: High Projection confidence: Medium

The compiler created a peeled loop because one of the memory accesses in the source loop does not start at a data boundary. Align the memory access and tell the compiler your memory access is aligned. This example aligns memory using a 32-byte boundary:

```
array = (float *)_mm_malloc(ARRAY_SIZE*sizeof(float), 32);
// Somewhere else
__assume_aligned(array, 32);
// Use array in loop
```

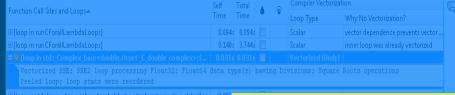
## Get Specific Advice For Improving Vectorization

Intel® Advisor – Vectorization Advisor





## 1. Compiler diagnostics + Performance Data + SIMD efficiency information



## 2. Guidance: detect problem and recommend how to fix it

Issue: Peeled/Remainder loop(s) present

All or some source loop iterations are not executing in the kernel loop. Improve performance by moving source loop iterations from peeled/remainder loops to the kernel loop. Read more at <u>Vector Essentials</u>, <u>Hillipping Full Vector</u>.

Recommendation: Align memory access

Projection confidence: Medium

The compiler created a peeled loop because one of the memory accesses in the source loop does not start at a data boundary. Align the memory access and tell the compiler your memory access is aligned.

This example aligns memory using a 32-byte boundary

3. "Accurate" Trip Counts + FLOPs: understand utilization, parallelism granularity & overheads

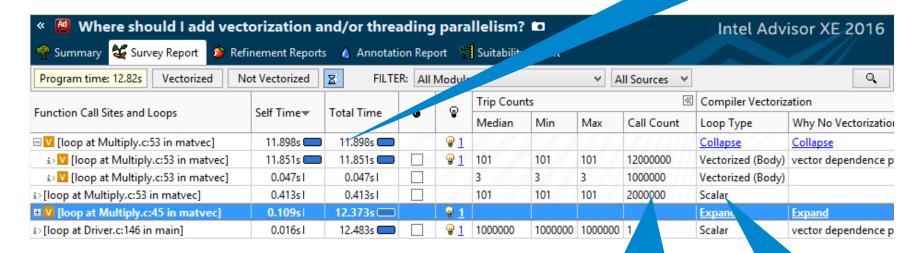
Total Time	Trip Counts						
	Median ▲	Min	Max	Iteration Duration	Call Count		
3,151s 📟	1	1	1	3,1509s	1		
0,440s I	1	1	1	< 0,0001s	2408000		
0,010s1	§ 1	1	2	< 0,0001s	207596		
0,010s1	½ 2	1	9	< 0,0001s	1173619		
0,010s1	₹3	1	5	< 0,0001s	1312315		

SIZE\*sizeof(float), 32);

## Critical Data Made Easy

#### **Loop Trip Counts**

Knowing the time spent in a loop is not enough!



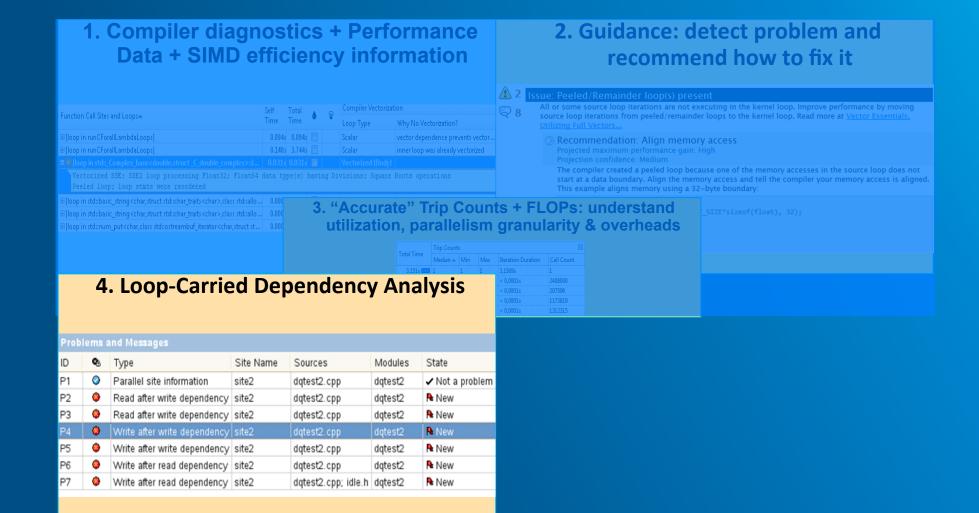
1.1 Find Trip Counts
Find how many iteration are executed.

Command Line

Check actual trip counts

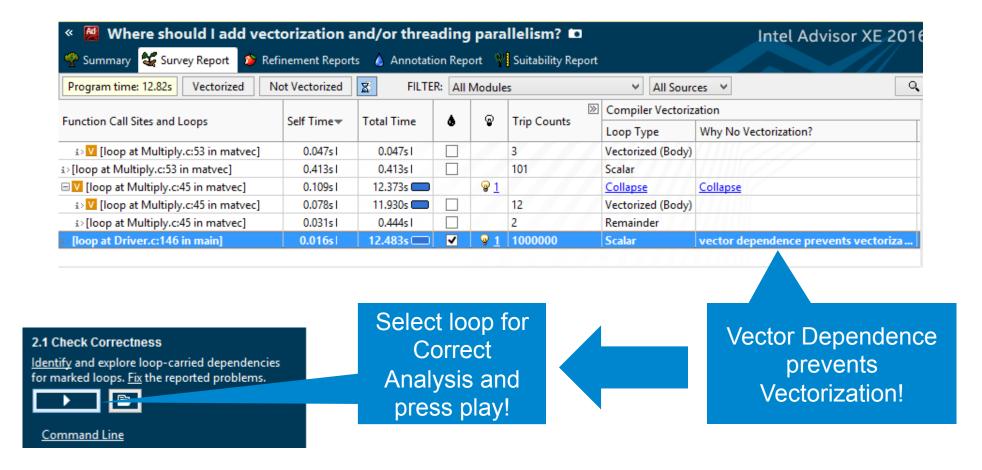
Loop is iterating 101 times but called > million times

Since the loop is called so many times it would be a big win if we can get it to vectorize.



#### Is It Safe to Vectorize?

#### Loop-carried dependencies analysis verifies correctness



## Data Dependencies – Tough Problem #1

Is it safe to force the compiler to vectorize?

#### Data dependencies

```
for (i=0;i<N;i++) // Loop carried dependencies!
A[i] = A[i-1]*C[i];// \text{ Need the ability to check if it}
// it is safe to force the compiler
```

#### Issue: Assumed dependency present

The compiler assumed there is an anti-dependency (Write after read - WAR) or true dependency (Read after write - RAW) in the loop. Improve performance by investigating the assumption and handling accordingly.

#### Enable vectorization

Potential performance gain: Information not available until Beta Update release Confidence this recommendation applies to your code: Information not available until Beta Update release

The Correctness analysis shows there is no real dependency in the loop for the given workload. Tell the compiler it is safe to vectorize using the restrict keyword or a <u>directive</u>.

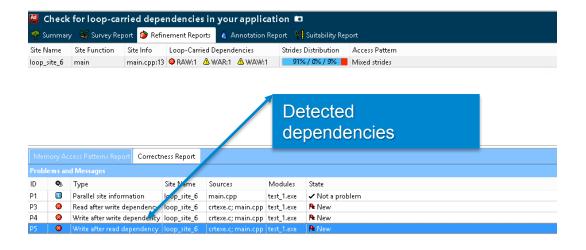
ICL/ICC/ICPC Directive	IFORT Directive	Outcome		
#pragma simd or #pragma omp simd	!DIR\$ SIMD or !\$OMP SIMD	Ignores all dependencies in the loop		
#pragma ivdep	!DIR\$ IVDEP	Ignores only vector dependencies (which is safest)		

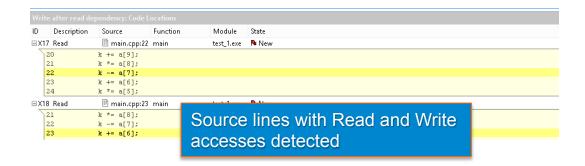
#### Read More:

- <u>User and Reference Guide for the Intel C++ Compiler 15.0</u> > **Compiler Reference** > **Pragmas** > **Intel-specific Pragma Reference** >
  - ivdep
  - omp simd

#### Correctness – Is It Safe to Vectorize?

#### Loop-carried dependencies analysis





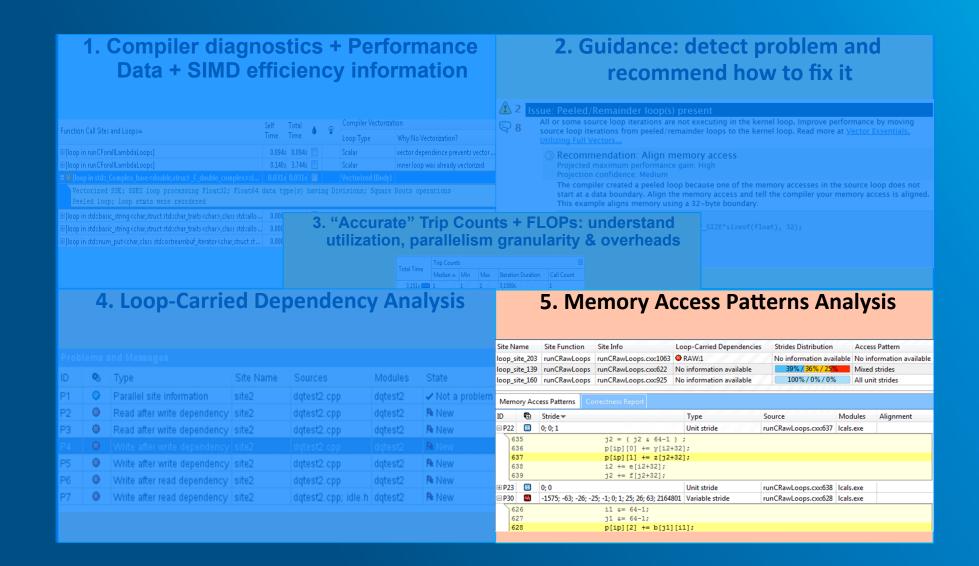
Received recommendations to force vectorization of a loop:

- 1. Mark-up the loop and check for the presence of REAL dependencies
- 2. Explore dependencies in more details with code snippets

In this example 3 dependencies were detected

- RAW Read After Write
- WAR Write After Read
- WAW Write After Write

This is NOT a good candidate to force vectorization!



## Non-Contiguous Memory – Tough Problem #2

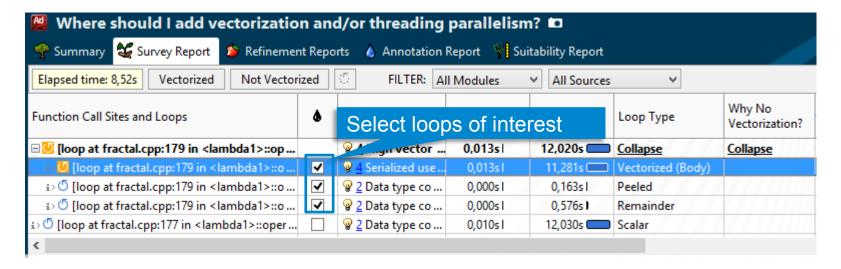
Potential to vectorize but may be inefficient

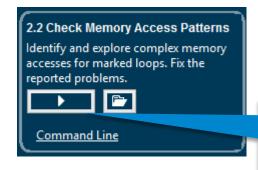
Non-unit strided access to arrays

Indirect reference in a loop

### Improve Vectorization

#### Memory Access pattern analysis



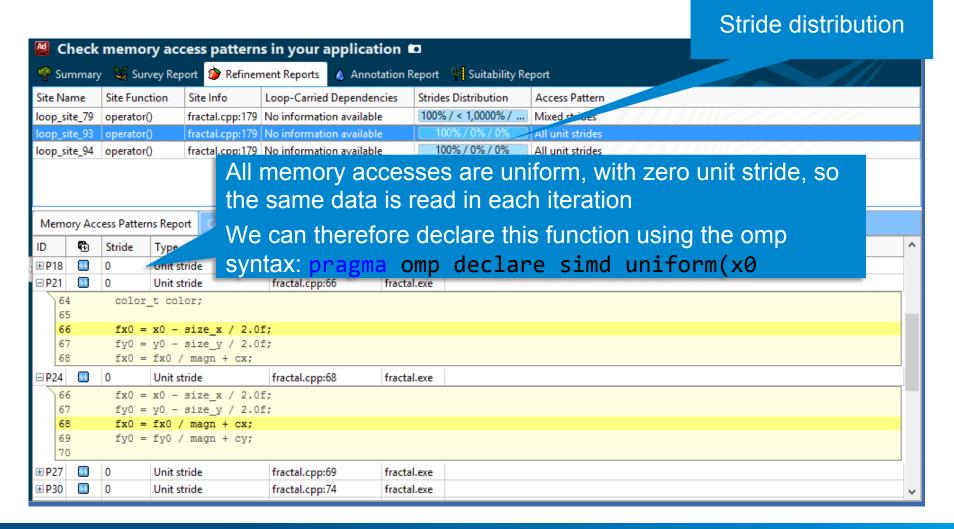


Run Memory Access Patterns analysis, just to check how memory is used in the loop and the called function



## Find vector optimization opportunities

Memory Access pattern analysis





### Advisor 2017 Update 2 Features

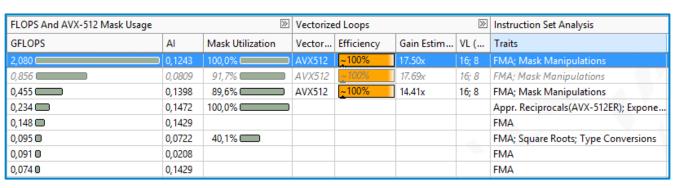
- 1. Cache aware Roofline
- 2. Improved Trip Counts and FLOPS
  - 1. Call Count metric for functions
- 3. Filtering by module
- 4. Re-finalization
- 5. Dynamic Instruction

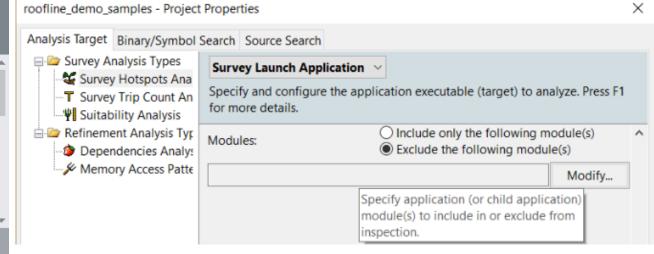
#### Mixes

1. -report survey -mix

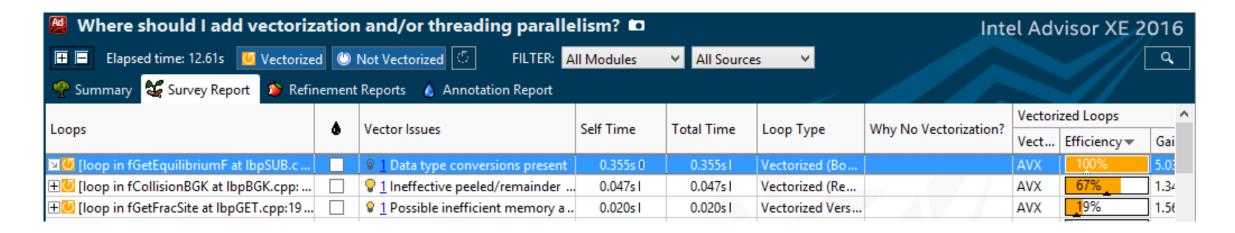






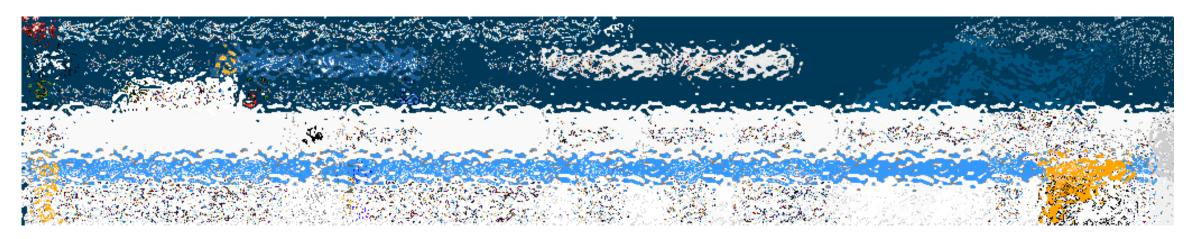


## Vectorized loops with high efficiency



Are we done??..

## Vectorized loops with high efficiency

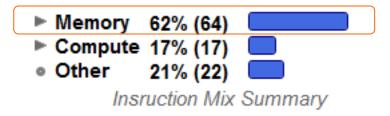


...It depends.

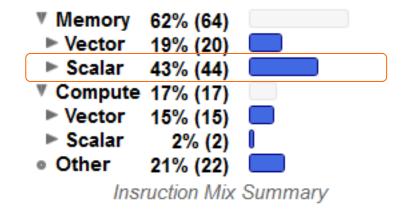
If code is not SIMD bound, then Speedup <= Vectorization Gain

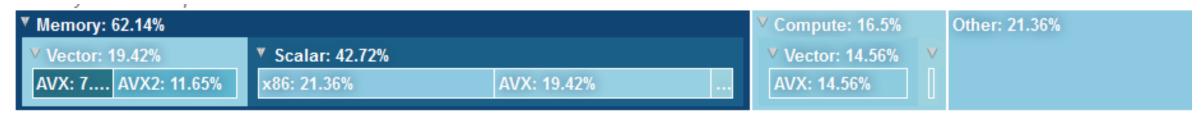
In addition(instead of) VPU-bound code could be Memory Bound

# Am I bound by VPU/CPU or by Memory? Quick and Dirty check with Survey Loop Analytics.

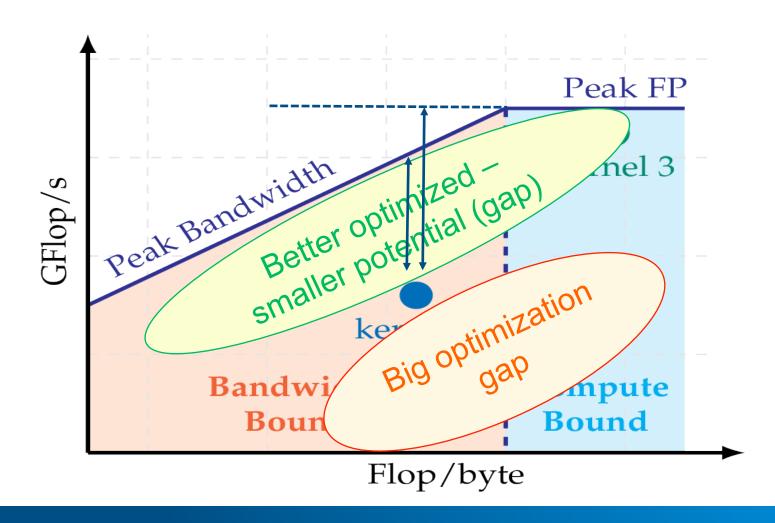


The types of instructions in your loop will be a rough indicator of whether your are doing more memory or computational work

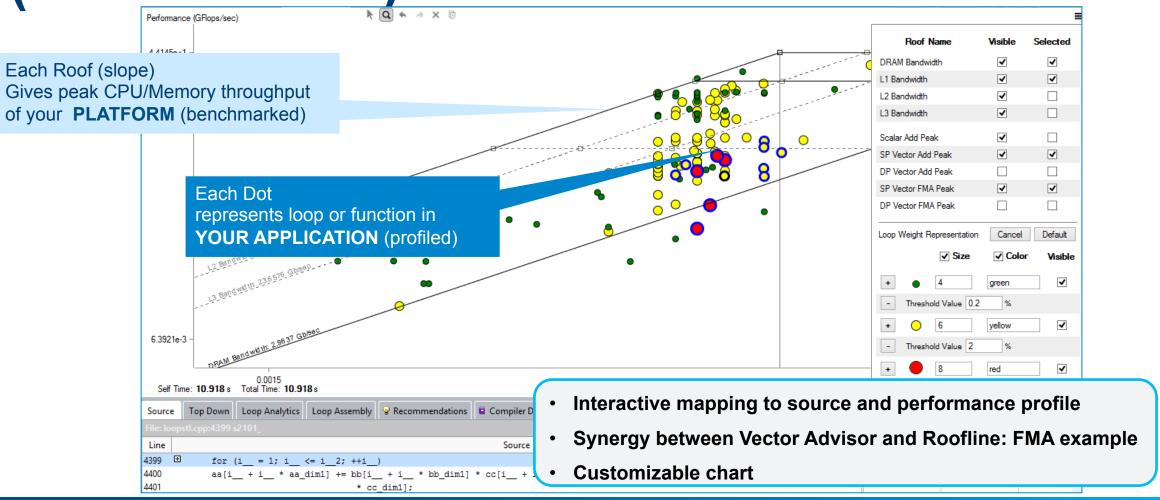




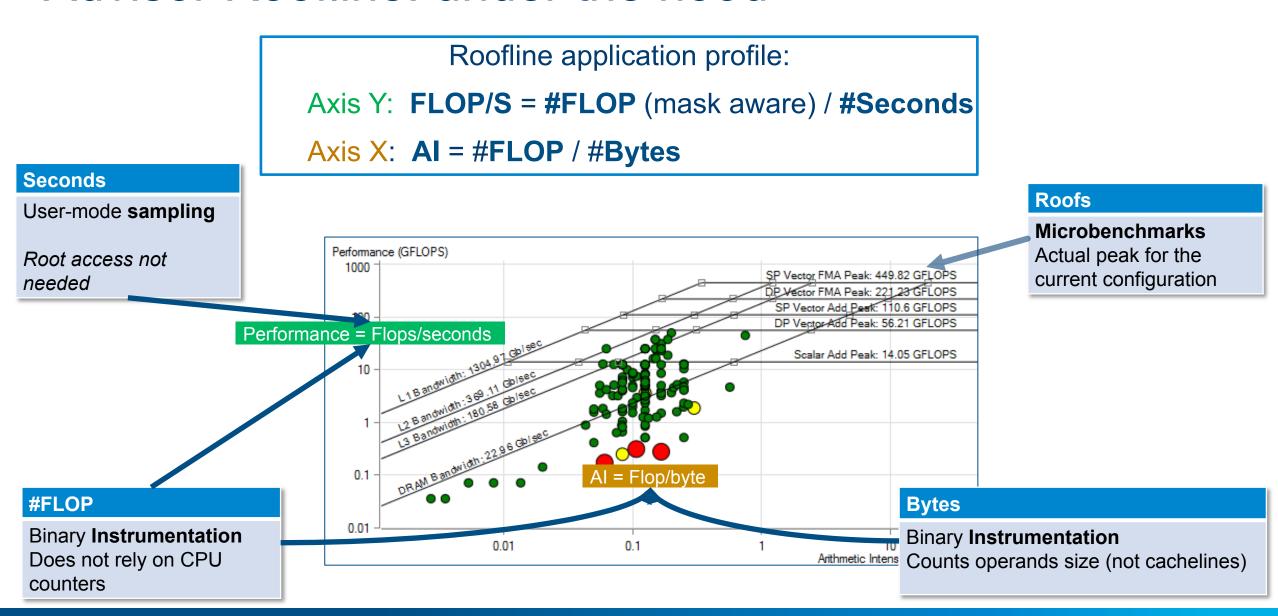
## Am I bound by VPU/CPU or by Memory? ROOFLINE ANALYSIS



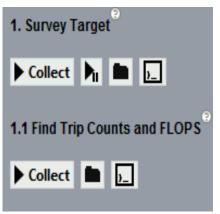
# Roofline Automation in Intel® (Vectorization) Advisor 2017



#### Advisor Roofline: under the hood

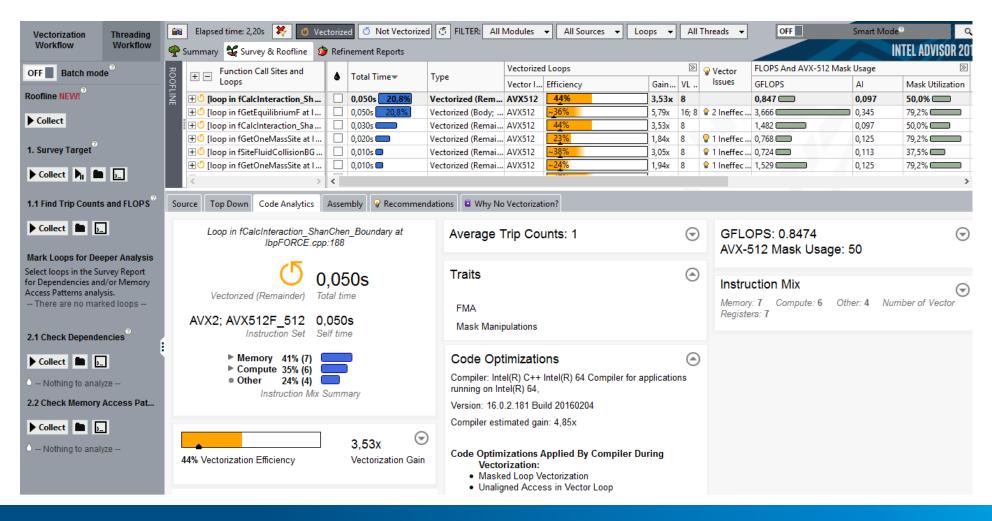


## Getting Roofline in Advisor

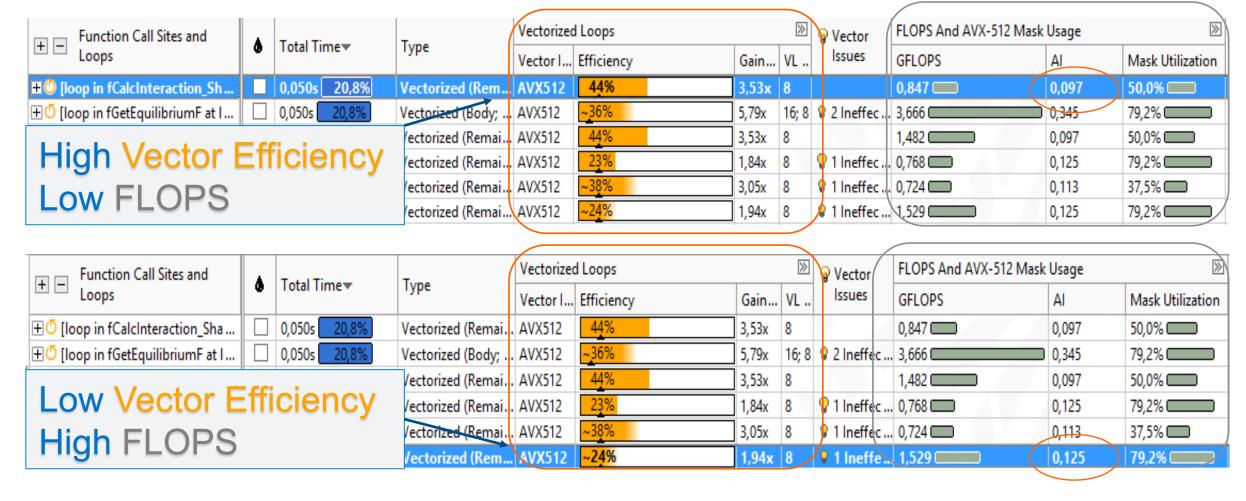


FLOP/S = #FLOP/Seconds	Seconds	#FLOP Count - Mask Utilization - #Bytes
Step 1: Survey - Non intrusive. Representative - Output: Seconds (+much more)		
Step 2: FLOPS  - Precise, instrumentation based  - Physically count Num-Instructions  - Output: #FLOP, #Bytes		

# Survey+FLOPs Report on AVX-512: FLOP/s, Bytes and AI, Masks and Efficiency



## General efficiency (*FLOPS*) vs. VPU-centric efficiency (Vector Efficiency)

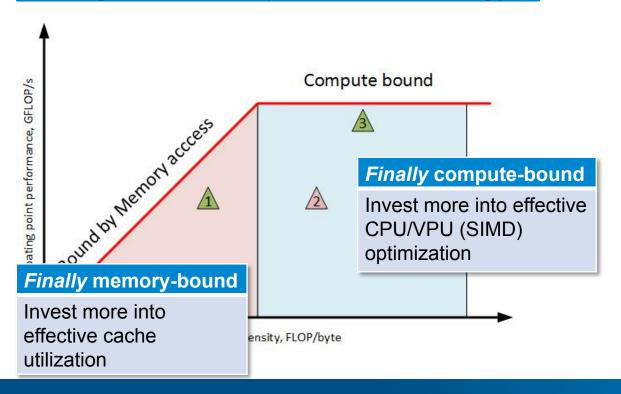


# Interpreting Roofline Data: advanced ROI analysis.

#### **Final** Limits

(assuming perfect optimization)

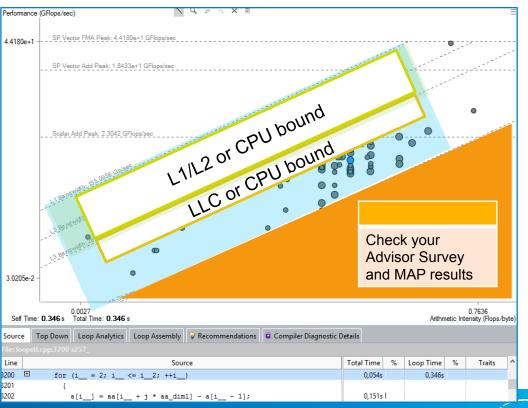
Long-term ROI, optimization strategy



#### **Current** Limits

(what are my current bottlenecks)

Next step, optimization tactics



## Command line usage

- advixe-cl -collect survey -project-dir ./your\_project -no-auto-finalize search-dir src=./srcPath -search-dir bin=./binPath -- ./yourExecutable
- advixe-cl -collect map -mark-up-list=10,12,15 -project-dir ./your\_project search-dir bin=./binPath -search-dir src=./srcPath -- ./yourExecutable
- advixe-cl -collect dependencies --project-dir ./your\_project --loops="loop-height=0,total-time>2" -- ./yourExecutable
- advixe-cl -report survey -project-dir ./yourProject --search-dir src:r=./src
- advixe-cl -collect survey -module-filter-mode=include -module-filter=AnalyzeMyApp.exe,AnalyzeThisToo.dll -project-dir MyProject -- AnalyzeMyApp.exe
- advixe-cl -collect survey -module-filter-mode=exclude -module-filter=DoNotAnalyze.so -project-dir MyProject -- MyApplication

#### Roofline access and how-to

- For 2017 Update 1
  - (!) Requires env variable set before running command line or GUI:

export ADVIXE\_EXPERIMENTAL=roofline

Starting from 2017 Update 2

Just available by default

# Roofline access and how-to command line example



```
(optional) > source advixe-vars.sh
(optional) > export ADVIXE_EXPERIMENTAL=roofline
```

1st pass
Obtain "Seconds"

1.1x overhead

```
> advixe-cl --collect survey -no-auto-finalize --project-dir ./your_project
-- <your-executable-with-parameters>
```

2<sup>nd</sup> pass
Obtain #FLOP count:
3x-5x overhead

```
> advixe-cl --collect tripcounts -flops-and-masks --project-dir ./
your project -- <your-executable-with-parameters>
```

Launch GUI

> advixe-gui ./your\_project



